

FIG. 1

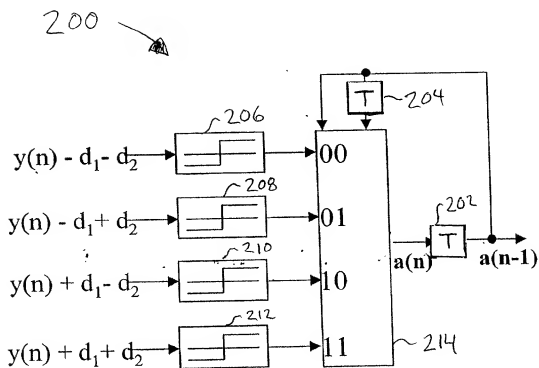
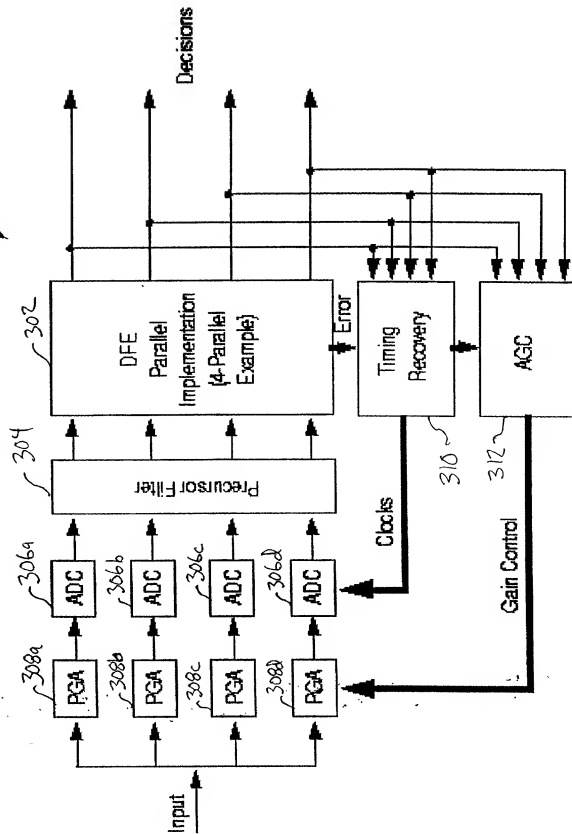


FIG. 2

300



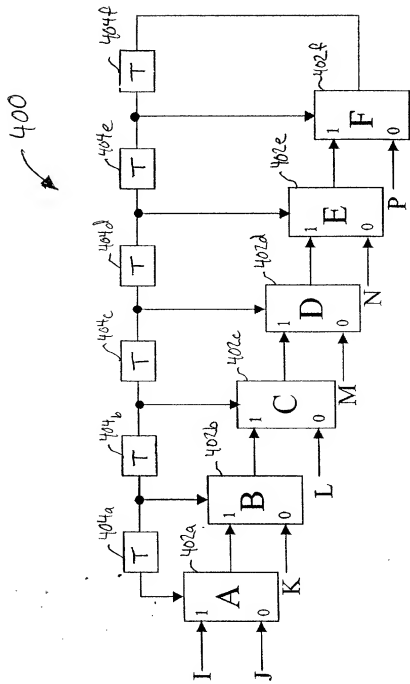


FIG. 4

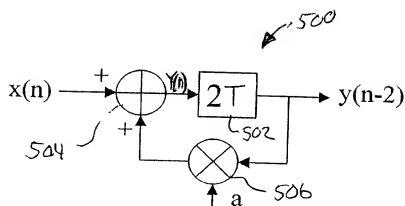


FIG. 5

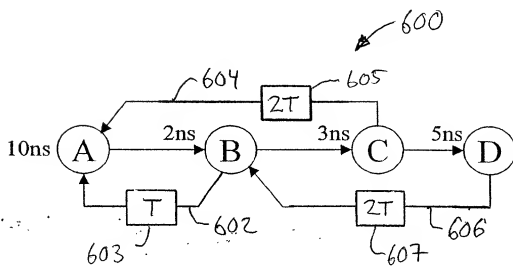


FIG. 6

700

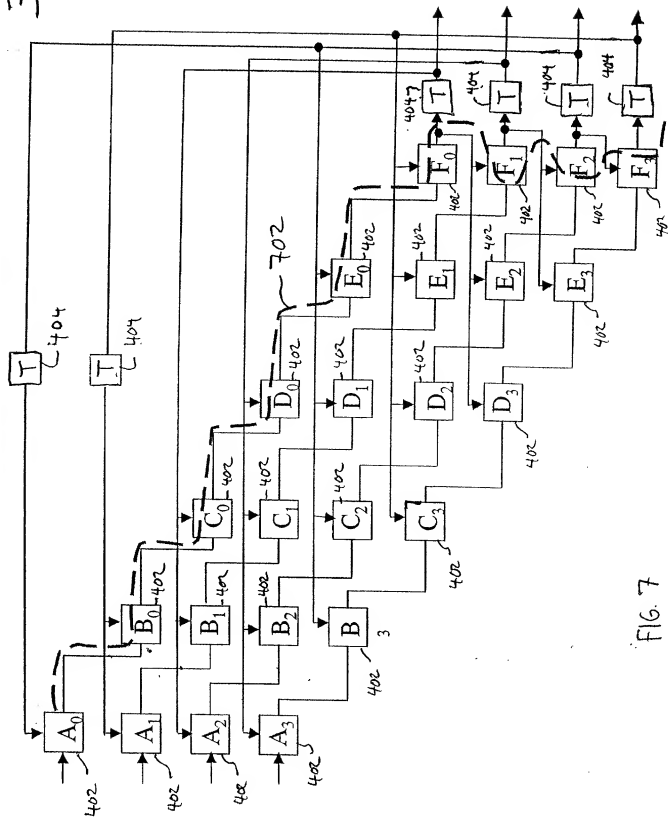


FIG. 7

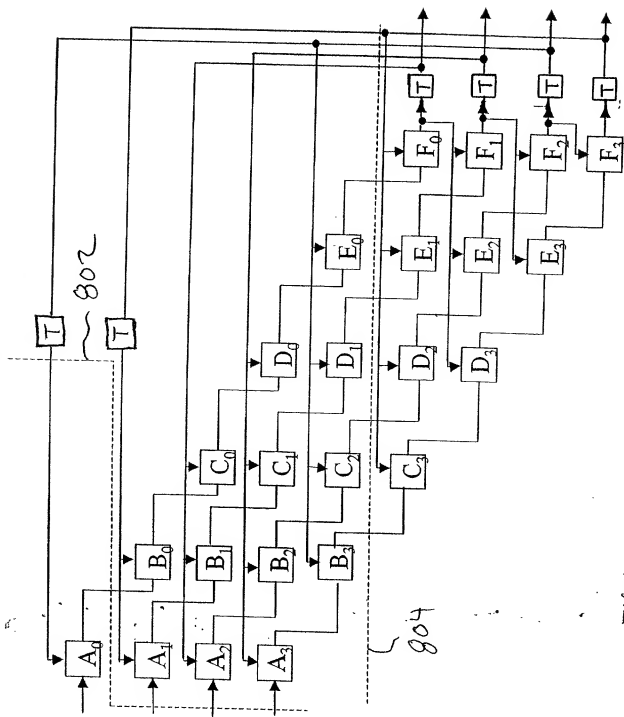


FIG. 8

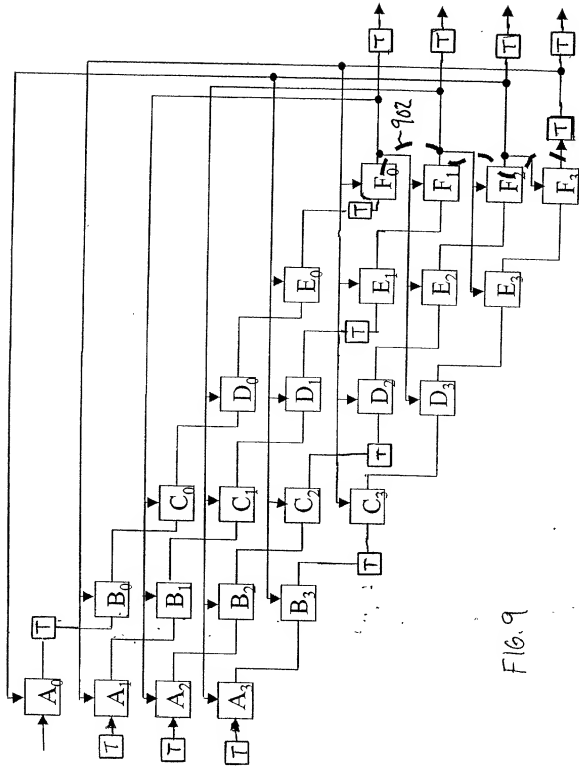


FIG. 9

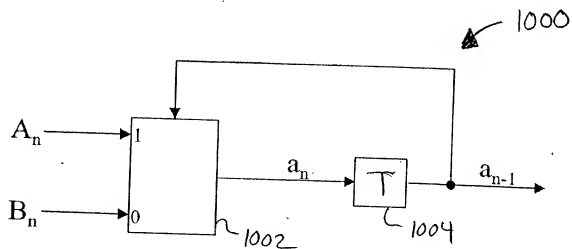


FIG. 10

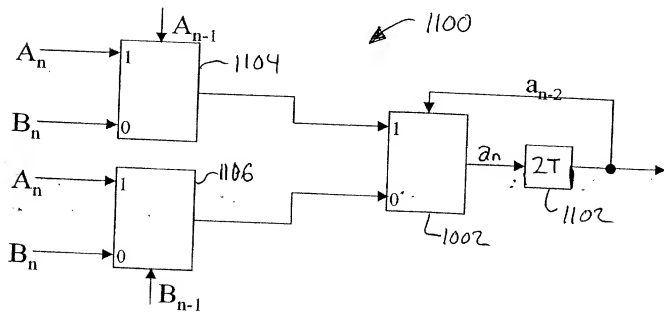


FIG. 11

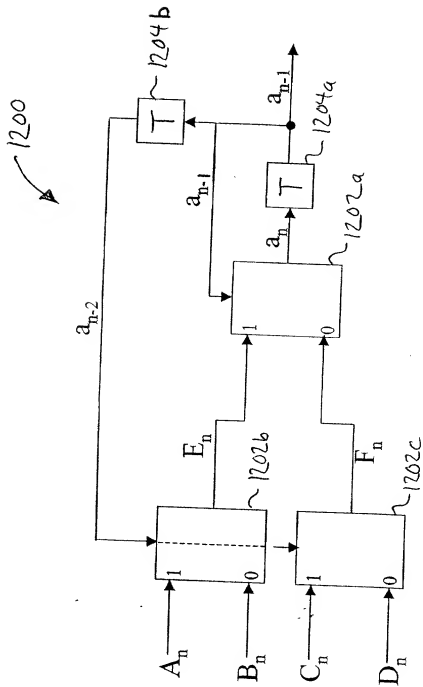


FIG. 12

1300

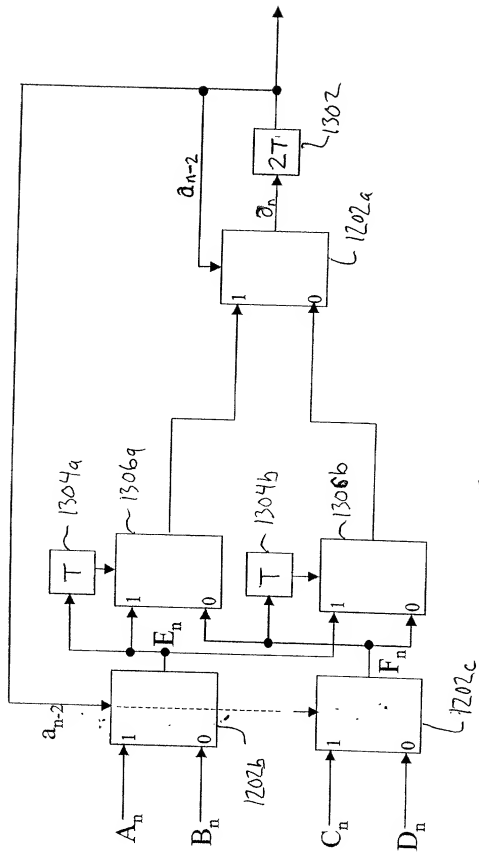
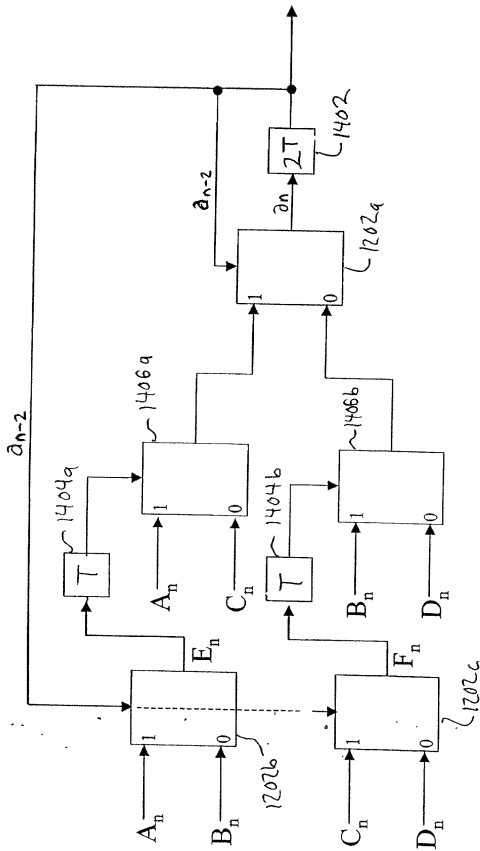


FIG. 13



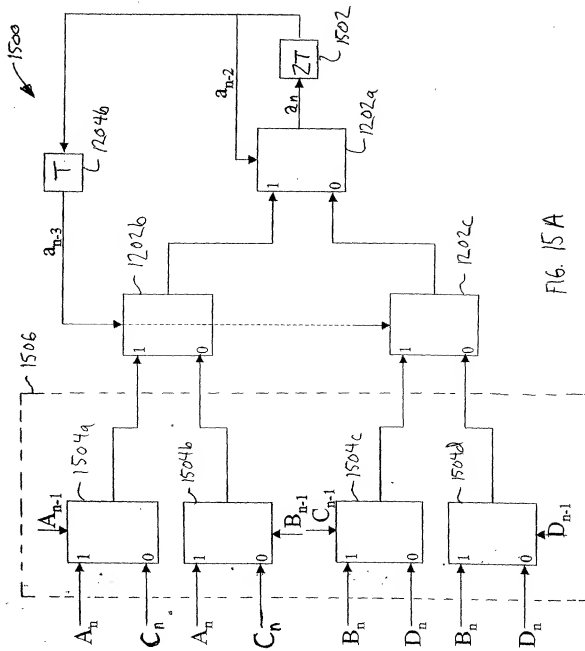


FIG. 15A

1550

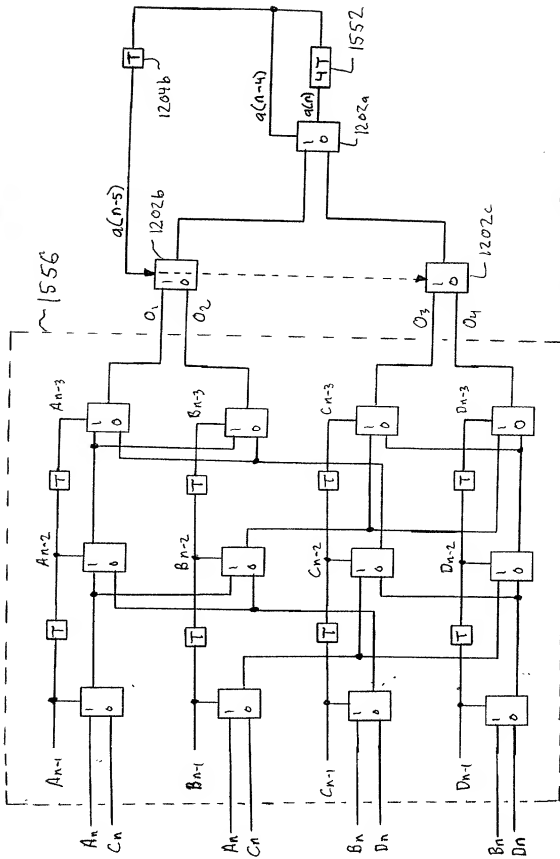


FIG. 15B

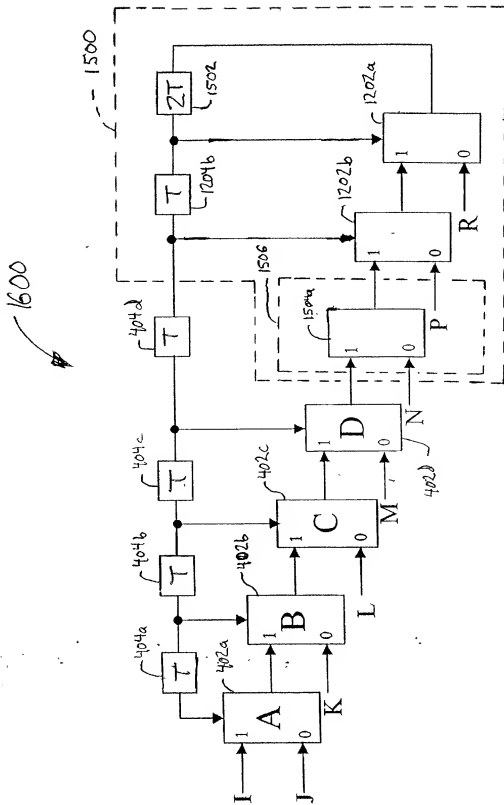


FIG. 16

1700

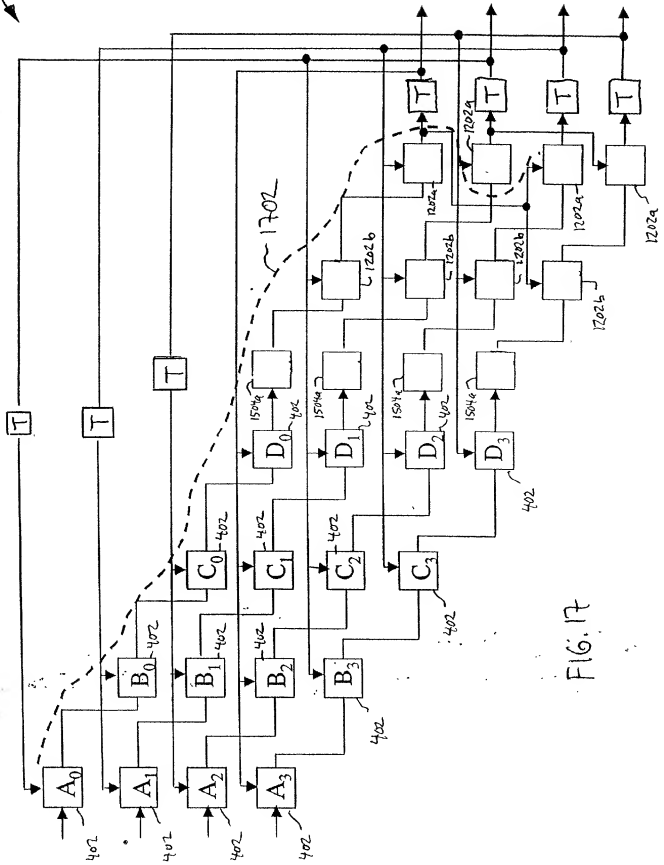


FIG. 17

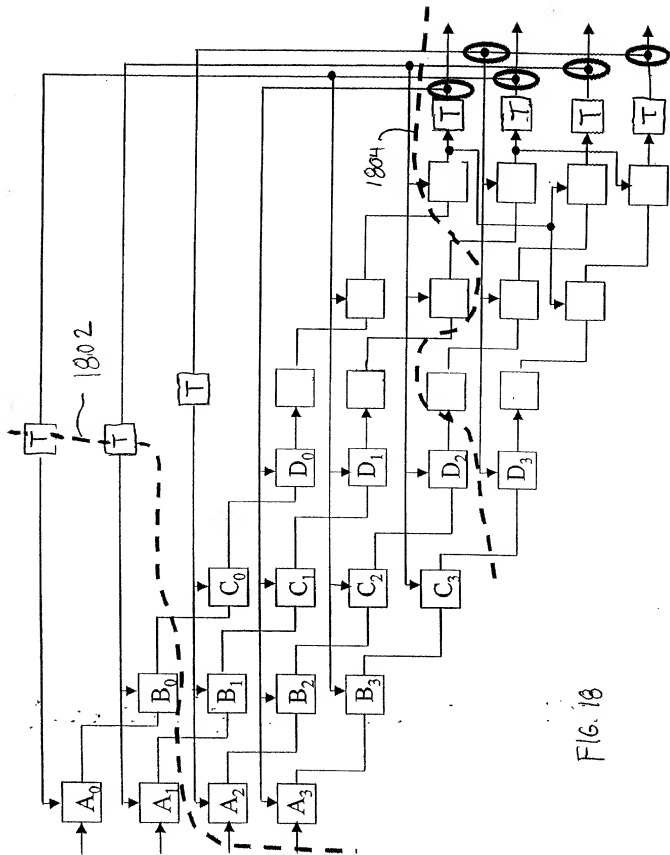
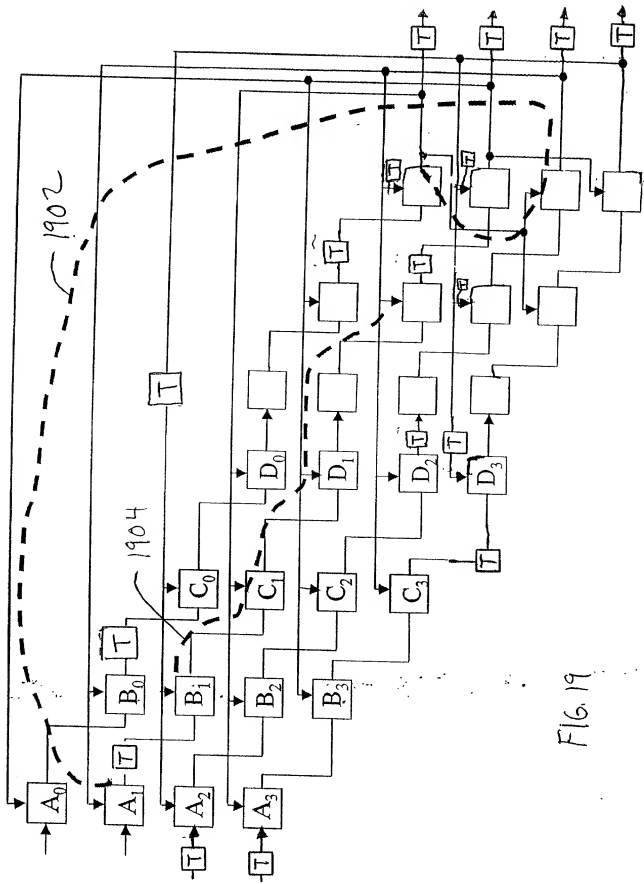


FIG. 18



2000

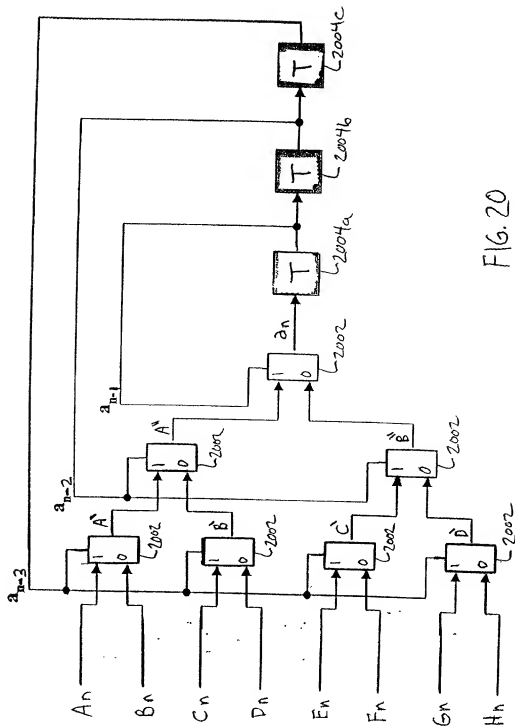


FIG. 20

208270*0165500T

2100

2104

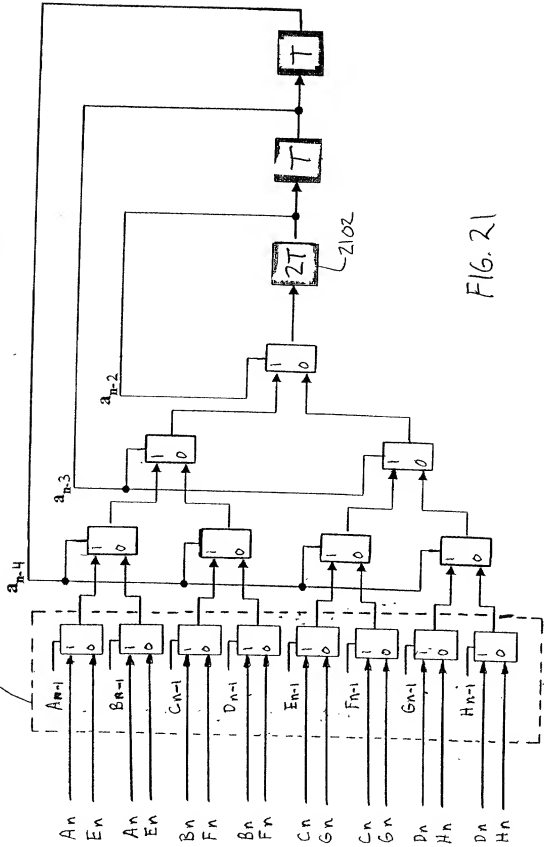


FIG. 21

SELECT A NUMBER OF INPUT VALUES TO BE PROVIDED TO A PIPELINED MULTIPLEXER LOOP DURING A CLOCK PERIOD OF OPERATION OF AN INTEGRATED CIRCUIT

2202

SELECT A NUMBER OF LOOK-AHEAD STEPS TO BE IMPLEMENTED AS A PART OF THE PIPELINED MULTIPLEXER LOOP

2204

IMPLEMENT THE PIPELINED MULTIPLEXER LOOP USING AT LEAST ONE DIGITAL LOGIC CIRCUIT, COMPRISING:

AN N -LEVEL LOOK-AHEAD NETWORK THAT CONVERTS THE NUMBER OF INPUT VALUES SELECTED IN STEP 2202 TO A PLURALITY OF INTERMEDIATE VALUES, WHEREIN N REPRESENTS THE NUMBER OF LOOK-AHEAD STEPS SELECTED IN STEP 2204,

A PLURALITY OF MULTIPLEXERS EACH HAVING A FIRST AND A SECOND INPUT PORT, AN OUTPUT PORT, AND A CONTROL PORT, THE PLURALITY OF MULTIPLEXERS ARRANGED TO FORM THE PIPELINED MULTIPLEXER LOOP, THE PIPELINED MULTIPLEXER LOOP HAVING AT LEAST A FIRST AND A SECOND STAGE, THE FIRST STAGE CONSISTING OF A FIRST MULTIPLEXER, AND THE SECOND STAGE CONSISTING OF A SECOND AND A THIRD MULTIPLEXER, THE PIPELINED MULTIPLEXER LOOP BEING COUPLED TO THE N -LEVEL LOOK-AHEAD NETWORK,

A FIRST COMMUNICATIONS LINK THAT COUPLES THE OUTPUT PORT OF THE SECOND MULTIPLEXER TO THE FIRST INPUT PORT OF THE FIRST MULTIPLEXER,

A SECOND COMMUNICATIONS LINK THAT COUPLES THE OUTPUT PORT OF THE THIRD MULTIPLEXER TO THE SECOND INPUT PORT OF THE FIRST MULTIPLEXER,

A FIRST FEEDBACK LOOP, HAVING A FIRST DELAY TIME, THAT COUPLES THE OUTPUT PORT OF THE FIRST MULTIPLEXER TO THE CONTROL PORT OF THE FIRST MULTIPLEXER, AND

A SECOND FEEDBACK LOOP, HAVING A SECOND DELAY TIME, THAT COUPLES THE OUTPUT PORT OF THE FIRST MULTIPLEXER TO THE CONTROL PORTS OF THE SECOND AND THIRD MULTIPLEXERS,

WHEREIN THE FIRST DELAY TIME IS AN INTEGER MULTIPLE OF THE SECOND DELAY TIME AND IS EQUAL TO $(N+1)$ TIMES A CLOCK PERIOD OF OPERATION OF THE INTEGRATED CIRCUIT.

2206

FIG. 22

10055910.012802

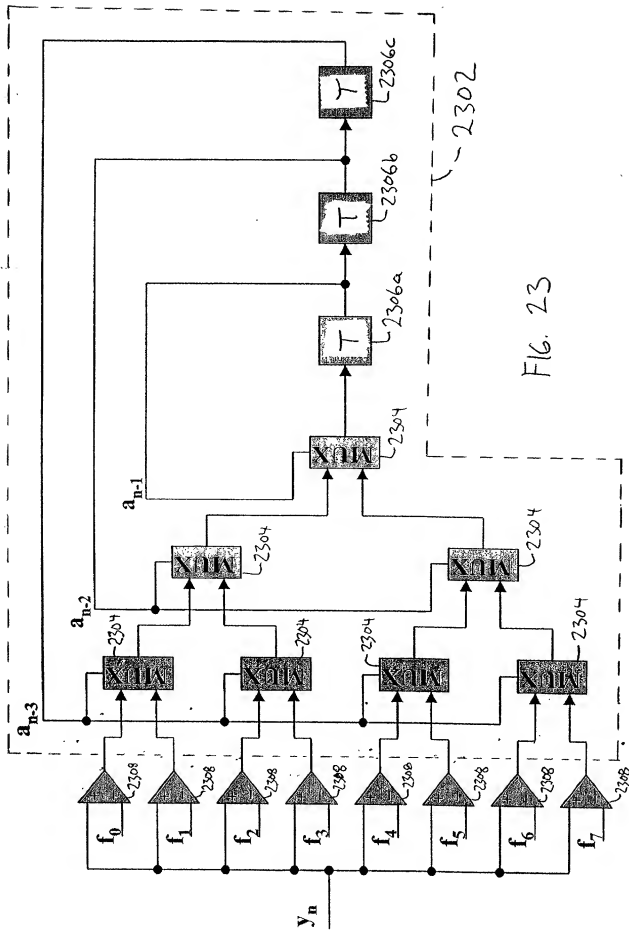


FIG. 23

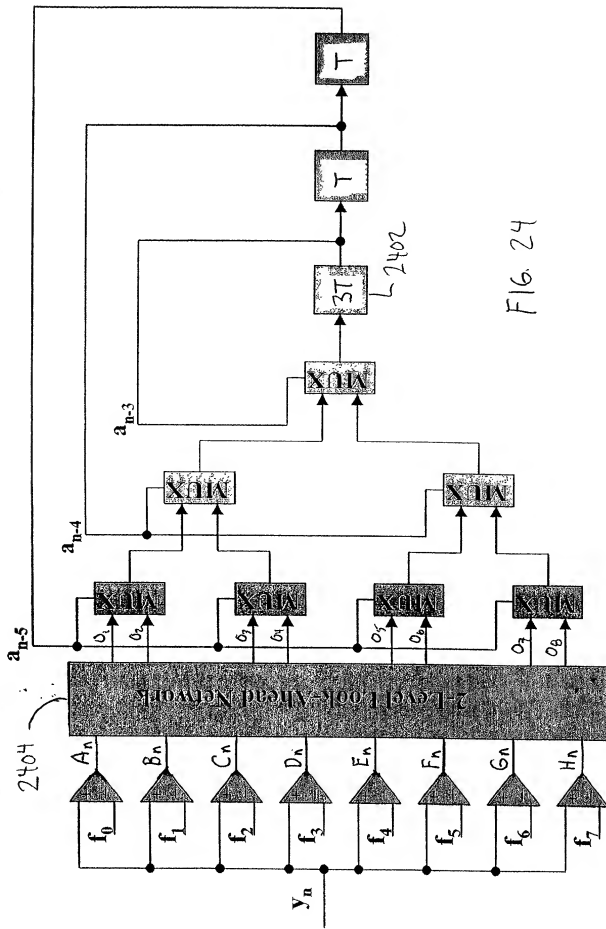


FIG. 24

2404

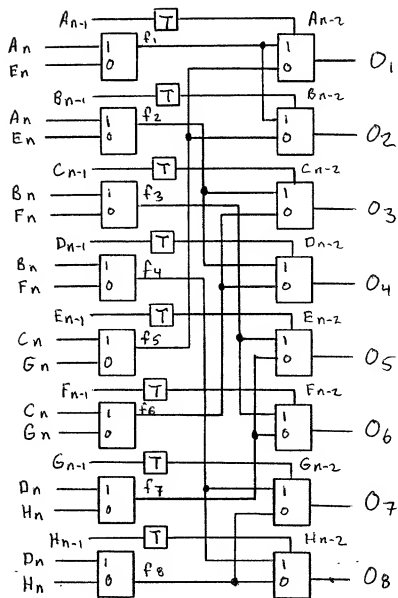


FIG. 25

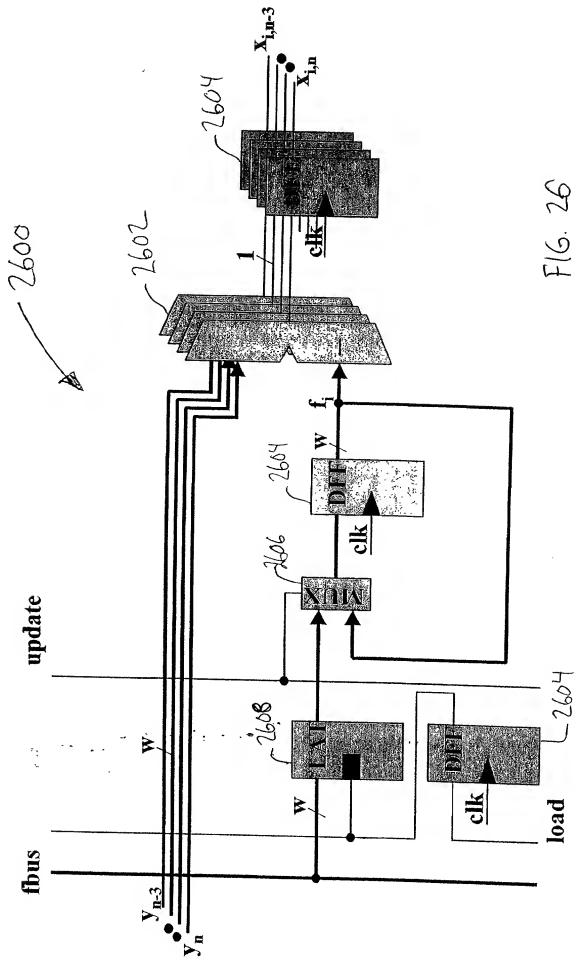


FIG. 26

2700

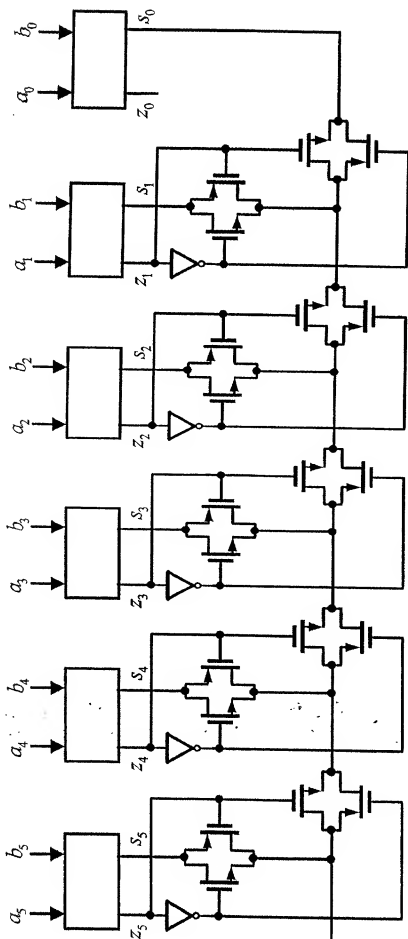
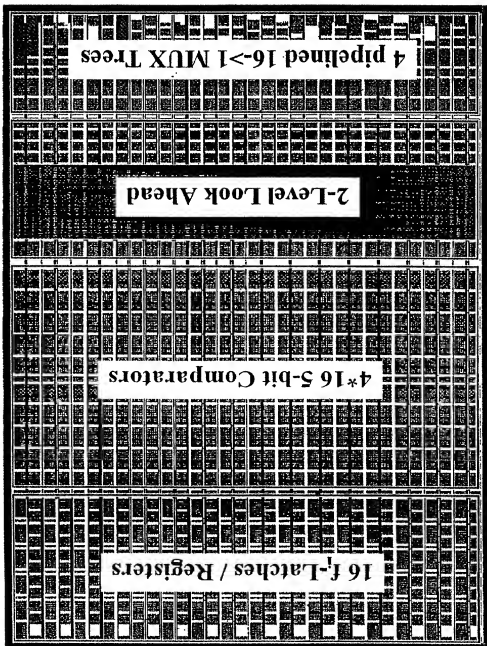


FIG. 27

10855910-012802

2800



F16. 28